

Serial No. 09/630,248

IN THE SPECIFICATION:

At page 1, in the "Related Applications:" paragraph, please change the paragraph to read as follows:

Sub E1
B1
Related Applications:

This is a continuation of Serial No. 08/930,648 filed January 20, 1998, now Patent No. 6,157,384. This application claims priority from PCT/JP97/00297 filed February 6, 1997, which claimed priority from Japanese Patent Application P8-020332 filed February 6, 1996.

At page 10, line 18 to 23, please delete the paragraph and insert in lieu thereof the following paragraph:

B2
The GPU 15 is a device on the main bus 1 functioning as a rendering processor. This GPU 15 interprets the drawing command sent from the main CPU 11 or main DMAC 13 as a command packet and performs rendering processing of writing pixel data in the frame buffer 18 from Z-values specifying depth and color data of all pixels

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B2
cont.
making up a polygon.

Please delete the paragraph from page 17, line 20, to page 18, line 6, and insert in lieu thereof the following paragraph:

B3
The data structure in the texture cache 33F, shown as an example in Fig. 4, is comprised of a tag area TAG made up of texture addresses, a storage area DATA having stored therein the necessary texture data and a flag L specifying that the texture data has not as yet been used. For employing the entry, having the flag L reset, the texture cache 33F reads in the texture data from the texture area of the frame buffer 18 to set its flag L. The drawing engine 33 reads out the corresponding texture data from the entry, the flag of which has been set, in order to perform drawing processing, and resets the flag L of the entry at a stage in which the drawing has come to a close and hence the texture data is no longer required.

Please delete the paragraph from page 30, line 25, to page 31, line 8, and insert in lieu thereof the following paragraph: